Notice of Allowability	Application No.	Applicant(s)	
	09/680,041	TAY, HIOK-NAM	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 10/26/2004*.

2. ☒ The allowed claim(s) is/are *1,4-11,13-16,19-25,27-45,48-64 (The claims are renumbered as 1-56)*.

3. ☒ The drawings filed on *05 October 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a faxed copy form Farshad Farjami on November 17, 2004.

2. The application has been amended as follows:

a. Claim 1 should be replaced as: A one time programmable solid-state device comprising:
a programmable memory unit embedded in a die within the one time programmable solid-state device;
a driver circuit that programs the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells; and
an access circuit that enables access to the programmable memory unit, wherein the access circuit is configured to drive one of the rows of the memory cells presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

b. Claims 2 and 3 are cancelled.

c. Claim 4: line 1, change "The one time programmable solid-state device of claim 3" to "The one time programmable solid-state device of **claim 1**".

d. Claim 5 should be replaced as: The one time programmable solid-state device of claim 1 wherein each of the memory cells is a capacitor.

e. Claim 6 should be replaced as: The one time programmable solid-state device of claim 1 wherein each of the memory cells is a transistor.

f. Claims 8 and 11: line 1, change "The one time programmable solid-state device of claim 2" to "The one time programmable solid-state device of **claim 1**".

g. Claim 12 is cancelled.

h. Claim 13 should be replaced as: The one time programmable solid-state device of claim 1 wherein at least one of the memory cells is permanently encoded.

i. Claim 14 should be replaced as: The one time programmable solid-state device of claim 13 wherein the at least one of the memory cells is permanently encoded by application of an effective voltage to a gate of the at least one of the memory cells, at least equal to a breakdown voltage of a gate oxide on a surface of the gate.

j. Claim 16 should be replaced as: The one time programmable solid-state device of claim 15 wherein each of the memory cells has a gate.

k. Claims 17 and 18 are cancelled.

l. Claim 19 should be replaced as: The one time programmable solid-state device of claim 16 wherein each of the memory cells is a capacitor.

m. Claim 20 should be replaced as: The one time programmable solid-state device of claim 16 wherein each of the memory cells is a transistor.

n. Claim 26 is cancelled.

o. Claim 27 should be replaced as: The one time programmable solid-state device of claim 16 wherein at least one of the memory cells is permanently encoded.

p. Claim 28 should be replaced as: The one time programmable solid-state device of claim 27 wherein the at least one of the memory cells is permanently encoded by application of an effective voltage to a gate of the at least one of the memory cells, at least equal to a breakdown voltage of a gate oxide on a surface of the gate.

q. Claim 29 should be replaced as: A method for programming a one time programmable solid-state device comprising:

writing, with a driver circuit, to a programmable memory unit embedded in a die within the programmable solid-state device locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells; and

accessing, with an access circuit, the one time programmable solid-state device wherein the access circuit is configured to drive one of the rows of the memory cells presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

r. Claim 37 should be replaced as: A method of data storage comprising:

identifying an address of a defective pixel in a photosensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device

storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device;

programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells; and

driving one of the rows of the memory cells presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

s. Claim 43: line 2, change "leakage current flowing through the gate oxide of at least one of the transistors" to "leakage current flowing through the gate of at least one of the transistors".

t. Claim 45 should be replaced as: A one time programmable solid-state device comprising:

a programmable memory unit embedded in a die within the one time programmable solid-state device;

means for programming the programmable memory unit with locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a

corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells; and

means for enabling access to the programmable memory unit, wherein the means for enabling access is configured to drive one of the rows of the memory cells presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

u. Claims 46 and 47 are cancelled.

v. Claim 48: line 1, change "The one time programmable solid-state device of claim 47" to "The one time programmable solid-state device of claim **45**".

w. Claim 49: line 1, change "The one time programmable solid-state device of claim 46" to "The one time programmable solid-state device of claim **45**".

x. Claim 51 should be replaced as: A one time programmable solid-state device comprising:

means for writing to a programmable memory unit embedded in a die within the programmable solid-state device locations of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells; and

means for accessing the one time programmable solid-state device, wherein the means for accessing is configured to drive one of the rows of the memory cells presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

y. Claim 57 should be replaced as: A one time programmable solid-state device comprising:

means for identifying an address of a defective pixel in a photosensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device;

means for storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device;

means for programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells; and

means for driving one of the rows of the memory cells in the two-dimensional array presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

z. Claim 65 is cancelled.

3. The following is an examiner's statement of reasons for allowance:

The following prior art shows the current state of the art to this patent application:

i. Heller (US Patent # 6,396,539) discloses a programmable memory (figure 2) in which controller unit has a driving and access unit (read as two different units) but does not disclose driving one of the rows of the memory cells in the two-dimensional array presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells, which is the core of the applicants' invention.

ii. Tomura et al. (US Patent # 5,521,639) discloses means for programming memory cells within the programmable memory unit with a first logic value or a second logic value, wherein each of the memory cells is associated with a corresponding pixel location, and wherein the first logic value represents a good pixel at the corresponding pixel location and the second logic value represents a defective pixel at the corresponding pixel location, wherein the memory cells have a number of rows of memory cells and a number of columns of memory cells (col. 6 lines 44-54) but does not disclose driving one of the rows of the memory cells in the two-dimensional array presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells.

As can be seen, the prior art does not teach or reasonably suggest a means for driving one of the rows of the memory cells in the two-dimensional array presently being read out to ground while tristating the columns of the memory cells and the other rows of the memory cells..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

4. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
November 19, 2004

TUAN HO
PRIMARY EXAMINER